Attorney Docket No. 030712-29

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant	:	Kazuaki Goto et al.	)	Confirmation No.: 3051
Serial No.	:	10/811,835	)	Examiner: Yelena Rossoshek
Filed	:	March 30, 2004	)	Art Unit: 2825
For	:	METHOD OF DESIGNING A CIRCUIT LAYOUT OF A SEMICONDUCTOR DEVICE	)	Date: March 30, 2009

APPEAL BRIEF

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Appeal is from the decision of the Examiner dated May 22, 2008, finally rejecting pending claims 1-3 and 10-13, which are reproduced as the Claims Appendix of this brief.

I. REAL PARTY IN INTEREST

The assignee of record and real party of interest is Oki Semiconductor Co., Ltd.

II. RELATED APPEALS AND INTERFERENCES

There are presently no appeals or interferences known to the Appellants, the Appellants' representative, or the assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3 and 10-13 stand finally rejected and are the subject of this appeal. Each of claims 4, 5, 14 and 15 are objected to as containing allowable subject matter, but depending from a rejected base claim. Claims 6-9 have been withdrawn from consideration by the examiner as being drawn to non-elected subject matter.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection. On November 24, 2008, Appellants submitted a Pre-Appeal Brief Request for Review. In response to this request, a USPTO review panel issued a communication to Appellants on December 30, 2008, which maintained the pending rejection and required submission of an appeal brief in accordance with 37 C.F.R. 41.37.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

As described starting in the "Background" section of the application, the invention relates to a method of designing a circuit layout of a semiconductor integrated circuit, for example, a large scale integration (LSI) device. The circuit layout design involves placement of functional circuit cells and spare cells called spare underground cells. After a circuit design change in logic is made, the spare cells are utilized to make the logic changes.

The claimed subject matter will now be described with reference to the independent claims:

Independent Claim 1

Claim 1 defines a method of designing a circuit layout of a semiconductor integrated circuit (e.g., see page 4, lines 21-22). The method comprises process of designing a logic function of the integrated circuit (e.g., see item 50 of Fig. 3, and page 4, lines 22-24), designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area (e.g., see item 52 of Fig. 3, and page 4, line 24 to page 5, line 2; Fig. 6, and page 6, lines 14-17), and providing a spare underground cell having no interconnect patterns and contacts (e.g., see Fig. 2 and page 4, lines 8-11). Claim 1 recites that the spare underground cell includes a functional element (e.g., see page 4, lines 14-20, and page 5, lines 9-22) and is inserted into the open area (e.g., see item 54 of Fig. 3 and page 5, lines 2-7; item 109 of Fig. 4; and page 8, lines 17-19). Design of a mask layout of the integrated circuit includes the logic cell and the spare underground cell is carried out in the next recited process (e.g., see item 56 of Fig. 3; and page 5, lines 6-8).

Independent Claim 10

Independent claim 10 recites a combination of features similar to claim 1, but requires more than one logic cell (e.g., see Fig. 6, and page 6, lines 14-17; page 6, line 6 (LSI design)) and more than one spare underground cell including more than one function element (e.g., see page 5, line 9 to page 6, line 1; and page 6, lines 9-10). Description in the specification of the remaining features recited in claim 10 is as pointed out above with respect to claim 1.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The single ground of rejection to be reviewed on appeal is as follows:

Claims 28, 33, 34 and 39 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Solomon et al. (U.S. Patent No. 6,446,248; hereinafter "Solomon").

VII. ARGUMENT

The rejection of claims 1-3 and 10-13 under 35 U.S.C. § 102(b) as allegedly being anticipated by Solomon, should be reversed.

Independent claims 1 and 10

MPEP § 2131 and the caselaw cited therein instructs that to anticipate a claim, a single source must contain all of the elements of the claim. The rejection based on the Solomon patent cannot stand because Solomon fails to either expressly or inherently disclose all the features recited in pending independent claims 1 and 10. More specifically, Solomon at least fails to disclose the processes of "providing a spare underground cell having no interconnect patterns and contacts," as recited in independent claim 1, and "providing a plurality of spare underground cells having no interconnect patterns and contacts," as recited in independent claim 10.

In setting forth the rejection, the Examiner alleges the claimed features of a spare underground cell "having no … contacts" are disclosed by Solomon's unconnected transistor terminals of the base cell 245. More specifically, the Examiner asserts:

> (within base cells 245 shown on the Fig. 3A, wherein base cell 245 includes plurality of transistors that have unconnected terminals (no interconnect and contacts) (col. 5, ll.10-16)). (Page 3, lines 5-7.)

In the "Remarks" section of the final Office Action, the Examiner further asserts:

> Solomon et al. teaches base cells 245 as shown on the Fig. 3A, wherein architecture of the base cell 245 depicted as plurality of **unconnected transistors**, wherein no interconnect patterns and contacts are shown, since each base cell 245 includes transistors that have **unconnected terminals** (col. 5, ll.10-16). Therefore Examiner believes that the term in the claims 1 and 10 'spare underground cell having no interconnect patterns and contacts' is equivalent to having **unconnected terminals** of base cell 245 (col. 5, ll.10-

11).[1] (Emphasis in original.) (Page 5, lines 14-16.)

It is respectfully submitted, however, that the forgoing statements by the Examiner are in error because one of ordinary skill in the art would understand that the description of "unconnected terminals," when taken in the context of Solomon's description of a base cell 245, refers to cell structure that includes contacts. First, one of ordinary skill in the art would understand that a "terminal" in the context of an electrical device is an element or device that facilitates electrical connection, especially when considering source/drain/gate terminals of a transistor. Indeed, the Solomon patent identifies, with respect to transistors M_{P1} to M_{PX} of a base cell 245, "metal traces 310_1 ... 310_4 and 312_1 ... 312_4 which are electrically coupled to the underlying poly-silicon with contacts in order to form terminals for the gates G_{p1} ... G_{p4} ..." (emphasis added) (see, column 5, line 66 to column 6, line 1, and Fig. 3B). Solomon also mentions contacts with regard to the other transistor terminals: metal 1 layer traces 320_1 to 320_4 and 322_1 to 322_4 for the source terminals of transistors M_{P1} to M_{PX}, at column 6, lines 3-5; metal 1 layer traces 330_1 to 330_4 and 332_1 to 332_4 for the drain terminals of transistors M_{P1} to M_{PX}, at column 6, lines 7-9; metal 1 layer traces 340_1 to 340_4 and 342_1 to 342_4 for the gate terminals of transistors M_{N1} to M_{NX}, at column 6, lines 27-29; metal 1 layer traces 350_1 to 350_4 and 352_1 to 352_4 for the source terminals of transistors M_{N1} to M_{NX}, at column 6, lines 32-34; and metal 1 layer traces 360_1 to 360_4 and 362_1 to 362_4 for the drain terminals of transistors M_{N1} to M_{NX}, at column 6, lines 36-38. Hence, the Solomon patent explicitly describes the terminals of the transistors M_{P1} to M_{PX} and M_{N1} to M_{NX} of the base cell 245, and explicitly discloses that these transistor terminals are electrically coupled with contacts. In view of this, the Examiner's assertions are in error because they directly contradict what is explicitly described in Solomon.

Furthermore, it is to be noted that the transistors M_{P1} to M_{PX} and M_{N1} to M_{NX}

[1] It is believed the Examiner uses the term "is equivalent to" to mean that the claimed process of "providing a spare underground cell having no interconnect patterns and contacts" reads on Solomon's unconnected transistor terminals of the base cell 245, and not equivalence as defined under 35 USC 112, sixth paragraph and/or the doctrine of equivalence.

of the base cell 245 are shown in schematic form in Fig. 3A (column 5, lines 17-18), and these transistors are shown in more detail in Fig. 3B (column 5, lines 44-45). In fact, Solomon explicitly describes representations of the base cell 245 in Fig. 3A as a "schematic drawing" of a preferred embodiment (column 5, lines 17-18) (i.e., generic n-type and p-type conductivity MOSFETs in which each of the MOSFETs is shown in a simple format indicating a gate (e.g., Gp1), source (e.g., Sp1) and drain (e.g., Dp1)). One of ordinary skill in the art would understand the schematic nature of the diagram of Figure 3A presents elements of the base cell 245 in a higher conceptual level than that of Fig. 3B, which shows a detailed physical layout of "the preferred base cell 245" (see, column 5, lines 44-45). With reference to Fig. 3B, the cell 245 clearly has contacts as indicated by the cross-hatched regions (see the legend, which explicitly indicates these regions as a "Contact"). As pointed out above, Solomon's description of Figure 3B explicitly describes these metal traces that are coupled to underlying elements via contacts to form terminals of the transistors of the base cell 245.

In the last paragraph of page 5 of the final Office Action, the Examiner asserts:

> It has to be noted that Applicant's representative cited description of the Fig. 3B, which is a physical layout of the base cell 245 and discloses further as a next stage: process of fabricating stage of the integrated circuit including the base cell, wherein Solomon et al. teaches fabrication stage of the integrated circuit design layout including adding metal layers 1 and 2 to the base cell 245 layout, which is shown on the Fig. 3B.

It appears the Examiner is attempting to show an existing difference in kind between base cells 245 shown in Fig. 3A and base cells 245 shown in Fig. 3B. However, there is no description in the Solomon patent to support such an allegation. Rather, Solomon describes a base cell 245 in both schematic format (i.e., Fig. 3A) and a physical layout of the schematic representation (i.e., Fig. 3B). It is respectfully submitted that one of ordinary skill in the art would understand Fig. 3B shows a more detailed representation of the base cell 245 shown in Fig. 3A.

To the extent it appears the Examiner also is alleging the metal 1 layer is not part of Solomon's base cell 245, the Solomon patent does not disclose, either explicitly or inherently, that the metal 1 layer forming terminals that are electrically connected to contacts is not a part of the base cell 245. As pointed out above, Solomon describes a base cell 245 as including metal 1 layer at least for forming transistor terminals. Also, Solomon discloses that the base cell 245 includes transistors with unconnected transistor terminals (see, column 5, lines 10-11). Since the Solomon patent makes it clear that these terminals are electrically connected to underlying device layers via contacts (see, column 5, line 66 to column 6, line 1; and column 6, lines 3-5, 7-9, 27-29, 32-34, and 36-38), it necessary follows that the base cell 245 of Solomon includes metal 1 layer. In fact, column 5, lines18-20 describe that the base cells 245 include a high voltage rail V_{DD} and a low voltage rail V_{SS}, which are shown in both Fig. 3A and Fig. 3B, and Fig. 3B indicates these voltage rails are composed of "Metal 1." Hence, a base cell 245 of Solomon includes the metal layer 1, which is used to form the transistor terminals that are electrically coupled to underlying transistor layers via contacts.

For at least the foregoing reasons, the Solomon patent not anticipate the claimed process of providing a spare underground cell having no contacts, as set forth in independent claim 1, and a plurality of these spare underground cells, as recited in independent claim 10. Accordingly, the Section 102(b) rejection of these independent claims is in error and should be reversed.

Claims 2, 3 and 11-13 depend from one of independent claims 1 and 10, and are therefore also allowable at least for the above reasons, and further for the additional features recited. Accordingly, it is respectfully requested that the rejection of claims 1-3 and10-13 under 35 U.S.C. § 102(b) be reversed.

While no further fees are believed to be due, the Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-4525.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

The following is a complete list of all claims on appeal:

1. A method of designing a circuit layout of a semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

designing a pattern layout of the integrated circuit so that the pattern layout includes a logic cell area and an open area;

providing a spare underground cell having no interconnect patterns and contacts;

inserting said spare underground cell into the open area, wherein the spare underground cell includes a functional element; and

designing a mask layout of the integrated circuit, the mask layout including the logic cell and the spare underground cell.

2. The method of designing the circuit layout according to claim 1, wherein the functional element comprises a D flip-flop, an inverter, a NOR circuit, and NAND circuit, an exclusive OR circuit and a latch circuit.

3. The method of designing the circuit layout according to claim 1, wherein inserting the spare underground cell comprises:

dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cell into the distributed open area.

10. A method of designing a circuit layout of a semiconductor integrated circuit, comprising:

designing a logic function of the integrated circuit;

designing a pattern layout of the integrated circuit so as to include a plurality of logic cells in a logic cell area and an open area;

providing a plurality of spare underground cells having no interconnect patterns and contacts;

inserting said plurality of spare underground cells into the open area, wherein each of the spare underground cells includes a plurality of functional elements; and

designing a mask layout of the integrated circuit, the mask layout including the logic cells and the spare underground cells.

11. The method of designing the circuit layout according to claim 10, wherein the functional elements includes a D flip-flop, an inverter, a NOR circuit, a NAND circuit, an exclusive OR circuit and a latch circuit.

12. The method of designing the circuit layout according to claim 10, wherein each of the spare underground cells has a same kind of the functional elements.

13. The method of designing the circuit layout according to claim 10, wherein inserting the spare underground cells comprises:

dividing the pattern layout into a plurality of block regions;

searching the open area from the block regions;

distributing the open area into the block regions; and

inserting the spare underground cells into the distributed open area.

IX. EVIDENCE APPENDIX

(None)

X. RELATED PROCEEDINGS APPENDIX

(None)